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**IN THE UNITED STATES PATENT & TRADEMARK OFFICE**

IN RE APPLICATION OF  
KUNIO YONENO

SERIAL NO: 10/717,644

GROUP ART UNIT: 2673

FILED: NOVEMBER 21, 2003

EXAMINER:

FOR: METHOD AND APPARATUS FOR ADJUSTING DOT CLOCK SIGNAL

**LETTER**

Mail Stop DD  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith is a European Office Action for the Examiner's consideration.

The reference cited therein was previously filed on November 21, 2003.

Respectfully submitted,

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File	84 66107
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ANSO	



Application No. 97 301 191.9 - 2205	Ref. 80.66107	Date 03.12.2003
Applicant SEIKO EPSON CORPORATION		

**Communication pursuant to Article 96(2) EPC**

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(1) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

**of 4 months**

from the notification of this communication, this period being computed in accordance with Rules 78(2) and 83(2) and (4) EPC.

One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (Rule 36(1) EPC).

**Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Article 96(3) EPC).**



**DUE DATES  
NOTED**

13/4/04

**WOLFF L R**  
Primary Examiner  
for the Examining Division

Enclosure(s): 4 page/s reasons (Form 2906)



Bescheid/Protokoll (Anlage)		Communication/Minutes (Annex)		Notification/Procès-verbal (Annexe)	
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The examination is being carried out on the **following application documents**:

Text for the Contracting States:

DE FR GB NL

**Description, pages:**

1-67 as originally filed

**Claims, No.:**

1-68 as originally filed

**Drawings, sheets:**

1/41-41/41 as originally filed

1.). The following document is referred to in this communication; the numbering will be adhered to in the rest of the procedure:

*Refd. ....  
11-21-03*  
D1: EP-A-0 577 841 (FANUC LTD.) 12 January 1994

2.). The present application does not meet the requirements of Article 52(1) EPC, because the subject-matter of the method claim 1 and its associated device claim 16 is not novel in the sense of Article 54(1) and (2) EPC.

The document D1 discloses (the references in parentheses applying to this document) a method of automatically adjusting the phase of sampling clocks for a video signal (column 2 lines 34-38). The disclosed method defines the steps of:

- sampling the video signal by a plurality of clock signals having different phase relationships (column 2 lines 39 - 48), then obtaining plural set of image data (column 3 line 1 to 14).
- carrying out a predetermined operation for each set of image data to obtain an index, and to determine a desirable phase based on this index value (column 3 line 15 to 30).
- applying an optimum delay to the clock signal to have the desirable phase (column 3 line 30 to 45).

3.). Therefore the Examining Division agrees with the objection put forward by the Search Division as to lack of unity (Article 82 EPC). In fact, bearing in mind the



state of the art referred to above, the application appears to comprise five different concepts characterised by special technical features varying from one concept to the next. The reasons for the objection are as follows:

The first concept is defined in claims 1-5, 12-16, and 47-55. The problem to be solved by this first concept is how to adjust easily and automatically the phase of the dot clock signal of a flat display panel where said dot clock signal is regenerated starting from the horizontal synchronisation signal of the analog video signal to be digitized, so that meaningful analog video signal is sampled and visual artifacts are avoided, typically caused by sampling during transient periods (see the first embodiment description from page 17 line 17 up to page 27 line 2, illustrated with the figures 1 to 10).

The technical features involved by the first concept to solve this said problem is to use several clock signals generated from the horizontal synchronisation signal but having different phases. Then, a video line is stored and a predetermined function called function phase-related index of the sampled values is calculated. This phase related index function is a function indicating the sharpness of the line image under test, the best phase for the dot clock signal being deduced when the best sharpness is obtained, then, a delay circuit sets the phase accordingly.

The other concepts concern also a flat display panel where the dot clock signal has to be regenerated starting from the horizontal synchronisation signal of the analog video signal to be digitized, so that the same problem of avoiding visual artifacts has to be solved:

-The second concept (claims 6-11, 49-55) is to use a sampling clock generated at frequency slightly different than a normal one (the horizontal synchronisation signal frequency is multiplied by a factor) such that a linear increased phase deviation is obtained. Then, the image is divided in a plurality of data blocks, so that, regular increased phases are applied to those blocks. A phase related index is calculated for each block and the obtained maximum index is selected indicating the best phase for the dot clock signal (see the second embodiment, description from page 27 line 5 up to page 35 line 24, illustrated with the figures 12 to 16).

-The third concept (claims 17-26, 56-60) is to determine automatically the effective length of the lines of an image (pixel number per line) in order to deduce the actual frequency factor to be applied to the horizontal



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synchronisation signal frequency value, therefore sampling the video image correctly (see the third embodiment, description from page 35 line 27 up to page 46 line 11, illustrated with the figures 17 to 20).

-The fourth concept (claims 27-46, 56-57, 62, 63) is to determine the actual frequency factor to be applied to the horizontal synchronisation signal frequency value by determining the number of beats detected on a sampled data line (see the fourth and fifth embodiments, description from page 46 line 14 up to page 53 line 14, illustrated with the figures 17, 24 to 28).

-The fifth concept (claims 56-57, 61, 64-68) is to determine automatically the actual frequency factor (even if the line length is unknown) to be applied to the horizontal synchronisation signal frequency value by performing specific processing (correlation analysis operation of two image data respectively sampled by two dot clocks having different phases) (see the sixth and seventh embodiments, description from page 53 line 16 up to page 67 line 5, illustrated with the figures 29 to 39).

The technical features shared by all the concepts, which are mainly to implement a method for determining the best phase for the dot clock signal by means of calculating a specific function representing a characteristic of the image data (sharpness for example) to solve the said problem are known from document D1.

Neither the remaining technical features of the first concept, defined by the set of claims 1 to 5, 12 to 16, and 47 to 55, that is "applying a plurality of different delays to generate a plurality of dot clock signals and sampling the video signal to obtain plural sets of image data and selecting a delay among the plurality of delays corresponding to the extreme value of a function representing sharpness of said plural sets of image data",

nor any corresponding technical feature are present in the set of claims of the other concepts, so that the technical relationship between the subject-matter of claims 1 to 5, 12 to 16, and 47 to 55 and all the remaining claims required by Rule 30 is lacking, and the requirement for unity of invention referred to in Article 82 EPC is not fulfilled.

Since the applicant has not indicated on which invention searched by the Search Division the further prosecution of the application should be based, no further



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examination can be carried out for the time being (cf. the Guidelines, C-III, 7.11). The applicant is asked to state upon which invention further prosecution of this application should be based and to limit the application accordingly. Other inventions are to be excised from the claims, description and drawings if any.

The subject-matter to be excised may be made the subject of one or more divisional applications. The divisional applications must be filed directly at the European Patent Office in Munich or its branch at The Hague and in the language of the proceedings relating to the present application, cf. Article 76(1) and Rule 4 EPC. The time limit for filing divisional applications (Rule 25(1) EPC) must be observed.

- 4.). In view of the above objection it is not at present practicable to carry out a full examination of the application. The applicant is therefore requested to file suitable amendments upon which the further prosecution of the application is to be based.
- 5.) The following is also noted:
  - 5.1). If the applicant files an amended set of claims, the amended application shall meet the requirements of Article 84 EPC:  
Under Article 84 in combination with Rule 29(2) EPC an application may contain more than one independent claim in a particular category only if the subject matter claimed falls within one or more of the exceptional situations set out in paragraphs (a), (b) or (c) of Rule 29(2) EPC.  
Failure to do so, or to submit convincing arguments as to why the current set of claims does in fact comply with these provisions, will lead to refusal of the application under Article 97(1) EPC.
  - 5.2). The introductory part of the description should be adapted to any amended claims (Rule 27(1) (c) EPC).
  - 5.3). Amended claims should be in the two-part form and reference numerals should be added (Rule 29 (1) and (7) EPC).